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09/830,092	06/27/2001	Kazutaka Shibata	ROH-037	1091

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EXAMINER	
SONG, MATTHEW J	

ART UNIT	PAPER NUMBER
1722	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/830,092	Applicant(s) SHIBATA, KAZUTAKA	
	Examiner Matthew J. Song	Art Unit 1722	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,4,6,10,12,17-21 and 26-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,4,6,10,12,17-21 and 26-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 10, 12, and 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sekine et al (WO99/09595), where US 6,495,914 is used as an accurate translation, in view of Applicants admitted prior art (Admission) or Frye et al (US 5,898,223).

Sekine et al discloses bare chip devices **47** each including a plurality of semiconductor devices or IC chips with metal bumps **46** provided on the electrodes are placed and bonded on a base substrate **41** this reads on applicant's chip bonding step. Sekine et al also discloses connection posts (projections) **42** connected to electrodes **44** formed by etching, this reads on applicant's electrode forming step. Sekine et al also discloses epoxy resin **48** is filled in the recesses on the base substrate and coated over the projections and bare chip devices. The epoxy resin is flattened in its surface by grinding or polishing so that the connection posts **42,** and the metal bumps on the bare chip devices can be exposed, this reads on applicant's resin sealing step. Sekine et al also discloses the base substrate with module structures is cut along the centers between the adjacent surrounding walls into individual multi-chip module structures, this reads on applicant's cutting step ('914 col 9, ln 1-55 and Figs 4a-4d). Sekine et al also discloses

Sekine et al discloses a bare chip device **47,** including a plurality of semiconductor devices or IC chips bonded on a base substrate **41**. Sekine et al also discloses projections **42** and electrodes **44**, this reads on applicant's projection electrodes, and an epoxy resin coated over the projections and chips ('914 col 6, ln 5-40). Sekine et al does not disclose a first and second semiconductor chip, such that the first and second semiconductor chip defines a chip-on-chip structure.

In applicants admitted prior art, Admission teaches one of the structures capable of heightening the substantial integration density of a semiconductor device is a chip-on-chip structure. Admission also teaches in a semiconductor device having a chip-on-chip structure, a secondary ship is bonded face-down onto the surface of a primary chip and external connection electrodes are provided on the back side of the primary chip. Admission also teaches such a chip-on-chip structure is advantageous to obtain a high integration density of the elements. Admission also teaches semiconductor chips disposed below other semiconductor chips (page 4 of specification and Fig 19). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Sekine et al's chip device by using the chip-on-chip structure taught by Admission to obtain a high integration density of the elements.

In a method of making a chip-on-chip package, Frye et al teaches conventional chip-on-chip assemblies with chips supported by a chip having interconnection circuits on a support chip and bonding the chips with a solder bump and semiconductor chips disposed below other semiconductor chips (Fig 2 and col 3, 1-67). Frye et al also teaches chip on chip arrangements offer the advantage of utilizing the surface area of the support chip for interconnection routing (col 3, ln 15-25 and col 3, ln 45-50). It would have been obvious to a person of ordinary skill in

the art at the time of the invention to modify Sekine et al's chip device by using the chip-on-chip structure taught by Frye et al to utilize the surface area of the chip more effectively (col 3, ln 45-50).

Referring to claim 12, Sekine et al and Admission or Sekine et al and Frye et al teaches a plurality of chips and the semiconductor chip is bonded face down onto the solid device with an active surface of the semiconductor chip opposed to the solid device and substrate ('914 Figs 4a-4d).

Referring to claims 18-19, Sekine et al and Admission or Sekine et al and Frye et al teaches grinding the resin to expose the chip devices and projections ('914 col 6, ln 20-30), this reads on applicant's removing a surface layer section of the resin.

Referring to claim 20, Sekine et al and Admission or Sekine et al and Frye et al teaches the rear side of the multi-chip module structure is ground by grinding prior to the cutting step (col 6, ln 35-45).

Referring to claim 21, Sekine et al and Admission or Sekine et al and Frye et al teaches the projection electrodes 42 are formed with a height such that the top end of each projection electrode is between the height of the active surface of the chip and a height of an inactive surface of the chip (Figs 4a-4d).

3. Claims 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sekine et al (WO99/09595), where US 6,495,914 is used as an accurate translation, in view of Applicants admitted prior art (Admission) or Frye et al (US 5,898,223), as applied to claim 17, and further in view of Rai (JP 06-151701), an English Abstract has been provided.

The combination of Sekine et al and Admission or the combination of Sekine et al and Frye et al teaches all of the limitations of claim 29, as discussed previously, except the combination of Sekine et al and Admission or the combination of Sekine et al and Frye et al does not teach the semiconductor substrate includes a semiconductor wafer and the method is performed on a wafer level basis.

In a method of forming chip on chip devices, note entire reference, Rai teaches a wafer contains a number of semiconductor substrates, with a bonding part. Rai also teaches a semiconductor chip is bonded on the semiconductor substrate to from a plurality of chip on chip devices and the chip on chip devices are separated into individual pieces. Rai also teaches the man hours for manufacturing chip on chip devices can be reduced and cost can also be cut down (Abstract).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Sekine et al and Admission or the combination of Sekine et al and Frye et al by performing the method on a wafer level basis to reduce production time and cost, as taught by Rai.

4. Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sekine et al (WO99/09595), where US 6,495,914 is used as an accurate translation, in view of Rai (JP 06-151701), an English Abstract has been provided.

Sekine et al discloses bare chip devices **47** each including a plurality of semiconductor devices or IC chips with metal bumps **46** provided on the electrodes are placed and bonded on a base substrate **41** this reads on applicant's chip bonding step. Sekine et al also discloses

connection posts (projections) **42** connected to electrodes **44** formed by etching, this reads on applicant's electrode forming step. Sekine et al also discloses epoxy resin **48** is filled in the recesses on the base substrate and coated over the projections and bare chip devices. The epoxy resin is flattened in its surface by grinding or polishing so that the connection posts **42,** and the metal bumps on the bare chip devices can be exposed, this reads on applicant's resin sealing step. Sekine et al also discloses the base substrate with module structures is cut along the centers between the adjacent surrounding walls into individual multi-chip module structures, this reads on applicant's cutting step ('914 col 9, ln 1-55 and Figs 4a-4d).

Sekine et al discloses a bare chip device **47,** including a plurality of semiconductor devices or IC chips bonded on a base substrate **41**. Sekine et al also discloses projections **42** and electrodes **44**, this reads on applicant's projection electrodes, and an epoxy resin coated over the projections and chips ('914 col 6, ln 5-40). Sekine et al does not disclose a first and second semiconductor chip, such that the first and second semiconductor chip defines a chip-on-chip structure.

In a method of forming chip on chip devices, note entire reference, Rai teaches a wafer contains a number of semiconductor substrates, with a bonding part. Rai also teaches a semiconductor chip is bonded on the semiconductor substrate to from a plurality of chip on chip devices and the chip on chip devices are separated into individual pieces. Rai also teaches the man hours for manufacturing chip on chip devices can be reduced and cost can also be cut down (Abstract).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Sekine et al to form a plurality of chip on chip devices, as taught by Rai,

because chip on chip devices utilize the surface area of the chip more effectively and to obtain a high integration density of the elements.

5. Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egawa (JP 08-236692), where an English abstract and an English Computer translation (CT) have been provided, in view of Applicants admitted prior art (Admission) or Frye et al (US 5,898,223).

Egawa discloses a hybrid integrated circuit device, this reads on applicant's solid device, a semiconductor chip **16, 17** bonded onto a surface of the solid device, projection electrodes for external connection formed on the surface of the solid device **15**, and a protective resin layer **18,19** for sealing the surface of the solid device with head portions of the projection electrodes thereon exposed.

Egawa does not disclose a first and second semiconductor chip, such that the first and second semiconductor chip defines a chip-on-chip structure.

In applicants admitted prior art, Admission teaches one of the structures capable of heightening the substantial integration density of a semiconductor device is a chip-on-chip structure. Admission also teaches in a semiconductor device having a chip-on-chip structure, a secondary ship is bonded face-down onto the surface of a primary chip and external connection electrodes are provided on the back side of the primary chip. Admission also teaches such a chip-on-chip structure is advantageous to obtain a high integration density of the elements. Admission also teaches semiconductor chips disposed below other semiconductor chips (page 4 of specification and Fig 19). It would have been obvious to a person of ordinary skill in the art at the time of the

invention to modify Sekine et al's chip device by using the chip-on-chip structure taught by Admission to obtain a high integration density of the elements.

In a method of making a chip-on-chip package, Frye et al teaches conventional chip-on-chip assemblies with chips supported by a chip having interconnection circuits on a support chip and bonding the chips with a solder bump and semiconductor chips disposed below other semiconductor chips (Fig 2 and col 3, 1-67). Frye et al also teaches chip on chip arrangements offer the advantage of utilizing the surface area of the support chip for interconnection routing (col 3, ln 15-25 and col 3, ln 45-50). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Sekine et al's chip device by using the chip-on-chip structure taught by Frye et al to utilize the surface area of the chip more effectively (col 3, ln 45-50).

Referring to claim 12, the combination of Egawa and Admission or the combination of Egawa and Frye et al teaches the semiconductor chip is bonded face down onto the solid device with an active surface of the semiconductor chip opposed to the solid device and substrate (Figs 1-4 of Egawa and Fig 19 of Admission and Fig 2 of Frye et al).

6. Claims 3, 4, 6, 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sekine et al (WO99/09595), where US 6,495,914 is used as an accurate translation and an accurate translation can be provided upon request, in view of Fukasawa et al (US 6,455,920) and Ichikawa (JP 02-031437), where an English Abstract has been provided and an accurate translation can be provided upon request.

Sekine et al discloses all of the limitations of claim 3, as discussed previously, except a step for forming a back side resin layer on a back side of the semiconductor substrate and removing a back side resin through polishing or grinding from the semiconductor substrate.

In a method of forming a semiconductor device, Fukasawa et al teaches a semiconductor device **20A** with a resin layer **41** provided on the rear surface of the semiconductor chip. Fukasawa et al teaches the semiconductor chip is improved and problem damages in the bottom surface of the chip at the time of dicing the semiconductor wafer **51** into individual chips is eliminated (col 17, ln 35 to col 18, ln 67 and Figs 23-26). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify to modify Sekine et al with Fukasawa et al's resin layer on the bottom of the chip to eliminate damage to the bottom of the semiconductor chip during dicing.

The combination of Sekine et al and Fukasawa et al does not teach a back side grinding step of thinning the semiconductor substrate by removing the back side resin through polishing or grinding, from the semiconductor substrate.

In a method of packing a semiconductor chip, Ichikawa teaches a semiconductor chip is sealed in resin **21** and the rear side of the chip is subjected to grinding for a reduction in the packaging height. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify to modify the combination of Sekine et al and Fukasawa et al with Ichikawa's grinding of a resin layer to reduce the height and enhance the packaging density.

Referring to claim 3, the combination of Sekine et al, Fukasawa et al and Ichikawa teaches a step of forming a surface resin layer **48** ('914), a back side resin layer **41** ('920) and a back side grinding step ('437) and further polishing the back side of the semiconductor ('914 col

6, ln 35-40). It is also noted that further polishing is not patentable because splitting of one step into two, where the processes are substantially identical or equivalent in terms of function, manner and result was held to be not patentably distinguish the processes (Ex Parte Rubin 128 USPQ 159). The combination of Sekine et al, Fukasawa et al and Ichikawa teaches forming projections **43** ('914). The combination of Sekine et al, Fukasawa et al and Ichikawa teaches grinding or polishing ('914 col 6, ln 20-30).

The combination of Sekine et al, Fukasawa et al and Ichikawa is silent to the order of processing steps. The transposition of process steps where the processes are substantially identical or equivalent in terms of function, manner and result was held to be not patentably distinguish the processes ((Ex Parte Rubin 128 USPQ 159) and MPEP 2144.04).

The combination of Sekine et al, Fukasawa et al and Ichikawa is silent to the surface resin and the backside resin are substantially the same thickness. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Sekine et al, Fukasawa et al and Ichikawa by optimizing the thickness of the resin layer by conducting routine experimentation to obtain same.

The combination of Sekine et al, Fukasawa et al and Ichikawa is silent to bracing the substrate with the back side resin layer while the performing the surface grinding step so as to inhibit warpage of the substrate. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Sekine et al, Fukasawa et al and Ichikawa to perform the surface grinding step first; therefore the bracing the substrate with the backside resin layer would habe naturally flowed from the suggestion of the prior art. The fact that applicant has recognized another advantage which would flow naturally from following the

suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Referring to claim 4, the combination of Sekine et al, Fukasawa et al and Ichikawa teaches cutting the substrate after grinding ('914, col 6, ln 30-45).

Referring to claim 6, the combination of Sekine et al, Fukasawa et al and Ichikawa teahes the projections are embedded in the resin layer ('914 col 6, ln 5-40 and Figs 4a-4d).

Referring to claim 26, the combination of Sekine et al, Fukasawa et al and Ichikawa teaches cutting along the centers between the adjacent shield walls after grinding ('914 col 8, ln 40-60), this reads on applicant's cutting along cutting lines after completing the back side grinding step. The combination of Sekine et al, Fukasawa et al and Ichikawa is silent to polishing or grinding the surface resin layer such that the remaining surface layer has a thickness that is uniform. Uniformity is well known in the semiconductor art to be required to increase yield, which is desirable. Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Sekine et al, Fukasawa et al and Ichikawa by polishing or grinding the surface resin layer such that the remaining surface layer has a thickness that is uniform because increased uniformity is desirable in semiconductor manufacturing to increase yield.

Referring to claims 27 and 28, the combination of Sekine et al, Fukasawa et al and Ichikawa is silent to the surface resin layer is formed with uniform thickness and grinding the surface resin layer so that the heights of the plurality of projection electrodes is uniform. Uniformity is well known in the semiconductor art to be required to increase yield, which is desirable. It would have been obvious to a person of ordinary skill in the art at the time of the

invention to modify the combination of Sekine et al, Fukasawa et al and Ichikawa by forming a surface resin layer with uniform thickness and grinding the surface resin layer so that the heights of the plurality of projection electrodes is uniform because increased uniformity is desirable in semiconductor manufacturing to increase yield.

Response to Arguments

7. Applicant's arguments with respect to claims 10 and 12 have been considered but are moot in view of the new ground(s) of rejection.

8. Applicant's arguments, see page 8-9 of the remarks, filed 3/31/2005, with respect to the 112 first paragraph rejections of claims 26-28 have been fully considered and are persuasive. The rejection of claims 26-28 has been withdrawn in view of the drawings and specified portions of the specification.

9. Applicant's arguments filed 3/31/2005 have been fully considered but they are not persuasive.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Sekine et al teaches a wafer with a plurality of chip (Fig 3a) and a multi-chip module structure is cut into individual unit modules (col 9, ln 55-65). Admission and Frye teach forming a chip on chip device. A person of ordinary

skill in the art would have found it obvious to form the chip on chip device taught by Admission or Frye on the wafer before it is cut into individual units to improve productivity. Furthermore, the formation of chip on chip devices on a wafer level is taught by Rai (JP 06-151701), which shows that the combination would have been obvious to a person of ordinary skill in the art.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The Examiner admits Admission and Frye does not teach a cutting out step. Sekine et al discloses cutting the multi-chip structure into individual unit modules (col 9, ln 55-65 and col 8, ln 50-60). The combination would perform the chip on chip device formation prior to cutting to improve productivity.

Applicant's argument that Admission and Frye are unrelated to a chip on chip structure is noted but is not found persuasive. Admission and Frye teach chip on chip devices and methods of manufacturing ('223 col 2, ln 1-40 and page 4 of the specification).

Applicant's argument that Admission and Frye do not teach its formation on wafer or on a level wherein a cutting out step can be performed to take out individual pieces of chip on chip devices is noted but is not found persuasive. Sekine et al teaches forming a multi-chip on a substrate and cutting out to form individual chips (col 8, ln 40-60 and Fig 8f). Admission and Frye are not limited to only individual chips, as suggested by applicant. Admission and Frye teach forming a chip on chip structure by bonding a chip onto another chip to form a chip on chip structure. The teachings of Frye and Admission can be applied to the multi-chip structure of Sekine and would have been obvious to improve efficiency by forming multiple. Furthermore,

the formation of multiple chip on chip structure on a wafer and then cutting the wafer is known in the art, as evidenced by Rai (JP 06-151701).

Applicant's argument that obvious modification of the prior art of the order of process steps is not applicable is noted but is not found persuasive. The Examiner maintains that the selection of any order of process steps is held to be *prima facia* obvious, absent evidence of unexpected results (MPEP 2144.04). The case law applied by the Examiner *In re Rubin* is cited to show that the transposition, namely any order of process steps would have been obvious, absent evidence of unexpected results. The case law is applicable because the prior art teaches identical process steps to that which is claimed. The sole difference is the sequence of steps, which is not a patentable distinction unless the sequence results in unexpected results (MPEP 2144.04).

Applicant's argument that the order is critical is noted but is not found persuasive. The function of the steps and results of the steps, namely grinding away a resin layer to thin a resin layer are the same regardless of order. The function of the side resin layer is not relevant because the processes are equivalent in terms of function, manner and result; therefore the selection of the order would have been obvious to a person of ordinary skill in the art at the time of the invention.

Applicant's argument that there is not requirement to show an unexpected result is noted but is not found persuasive. The Examiner maintains that prior art teaches each of the claimed processes step and the prior art does not teach the order, however absent evidence of unexpected results, any order of processes would have been obvious (MPEP 2144.04), including the claimed order. A showing of unexpected results is required to properly traverse the rejection made by the Examiner.

Applicant's arguments against the case law of MPEP 2144.04 is noted but is not found persuasive. MPEP 2144.05 the selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results. The particularly cited case may apply to case outside the scope of the present invention, as suggested by applicant. However, selection of any order of processing steps is still *prima facie* obvious and generally applies to process claims.

Applicant's argument that if an unexpected results is to be considered in the present case, it should not be up to the Applicant to demonstrate that the result is unexpected is noted but is not found persuasive. The Examiner has made a proper rejection; therefore the burden shifts to the Applicant, which in the present case requires a showing of unexpected and new results, which has not been provided.

Applicant's argument that warpage is prone to occur when backside grinding is performed first is noted but is not found persuasive. Applicant has not shown that order of steps to be critical. Warpage is only prone to occur and conceivably may not occur given the various process conditions associated with warpage, namely layer thickness, temperature, material selection etc, which are all known in the art, as evidenced by Olsen et al ("Calculated stresses in multilayered heteroepitaxial structures") below. Therefore, the results are not unexpected and differences may not occur. Applicant has not show a difference, merely a tendency for a difference. Applicant's specification also suggests the order is non-critical by teaching both the backside grinder before front side and front side before backside grinding.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Takebashi et al (JP 59-092536) teaches applying a resin to a substrate and polishing (Abstract).

Olsen et al ("Calculated stresses in multilayered heteroepitaxial structures") teaches equations to determine bowing in a three layer composite, note entire reference.

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J. Song whose telephone number is 571-272-1468. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Duane Smith can be reached on 571-272-1166. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew J Song
Examiner
Art Unit 1722

MJS
July 7, 2005

ROBERT KUNEMUND
PRIMARY EXAMINER